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Engineering Note

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Project: CFT Axial
Doc. No: A981023A

Subject: Test Board for MCMs – Module Specification

Introduction

This note describes the basic features of an MCM test board which addresses the following needs:

1. A platform to exercise the analog and digital characteristics of the SIFT/SVX MCMs prior to mounting them permanently onto the CFT Axial cards.
2. A platform to test portions of trigger logic and timing before building the CFT Axial cards, with intent to make the first boards the final boards.
3. A platform for testing of PIC14000 microcontroller code.
4. A platform for testing a new 1553 interface.

A quick tour of the proposed features of this board are presented. Details of implementation will be added as the board design progresses.

Module Requirements

1. Board must be controlled via 1553 interface.
2. Board must receive test charge data from Bruce Knuteson's multi-DAC module.
3. Board must receive clocks and control signals from, and deliver SVX data to, the SVX Sequencer.
4. Board must house a Virtual SVX PLD.
5. Board must house a socket which can accept the SIFT/SVX MCM.
6. Board must provide prototype copy of all analog support functions associated with SIFT/SVX MCM.
7. Board must bring out MCM discriminator data to test SIFT functions.

Block Diagram and Feature List

The block diagram shown in Figure 1 provides all the functions necessary to satisfy the requirement list. Subsequent sections will describe the implementation of each block.

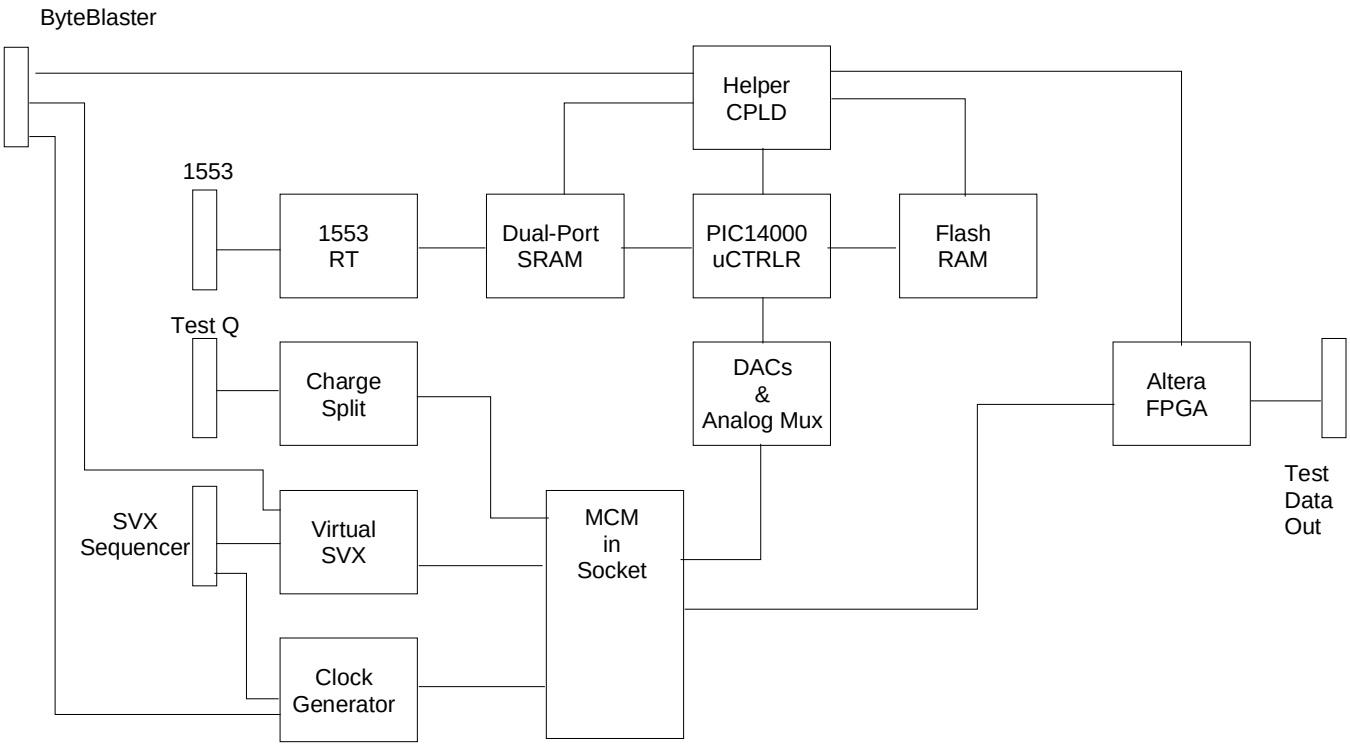

Figure 1

Clock Generator

The Clock Generator circuit provides a local 53 MHz clock and derived crossing clock (1 pulse every 7 ticks of the master clock) from an on-board oscillator. A clock detection circuit senses if the crossing clock is provided by the SVX Sequencer, and if so, the Clock Generator disables its own clock outputs and routes the SVX Sequencer clocks throughout the board. The Clock Generator also provides all the timing signals necessary to operate the SIFT and SVX by using delay lines driven by the crossing clock.

A counter within the Clock Generator issues a reset cycle to the MCM at fixed intervals based upon a counter driven by the crossing clock, or whenever a reset signal is issued by the SVX sequencer. The reset cycle will clear the SVX, reset all SIFT discriminators and insure that the MCM is not driven into saturation.

Virtual SVX

The Virtual SVX will not be the same Virtual SVX as described in the CFT technical design report, but a simple SVX emulator which allows the MCM test board to provide fixed data to the SVX Sequencer in response to SVX commands, to allow field testing of the SVX Sequencer. The data pattern provided by the Virtual SVX will be one of two types:

- a simple counting pattern with variations (such as provided by the Detector Emulation Module – see documentation at http://www-ese.fnal.gov/eseproj/svx/dem/dem.htm)
- A checksum of the data provided by the real SVX chip within the MCM.

Charge Split

The charge splitter will take the current pulses supplied by the DACs on Bruce's test module and convert them to charge pulses delivered to the SIFT inputs. Three-quarters of the charge signals will be severely attenuated to model signals from fibers, with the remaining quarter less attenuated to model preshower signals. A trigger/clock line will run from the Clock Generator back to the DAC module to insure that the charge pulses are delivered in sync with the rest of the board.

1553 RT Interface

This section will be the same circuit as described by Jamieson Olsen in his notes at http://d0server1.fnal.gov/users/jamieson/www/notes/index.html . The 1553 interface will provide up to 32 addresses in 1553 space, with the first two being a Base Address Pointer and a Data Window which allow access to every location within the dual-port RAM. The remaining 29 addresses will be directly translated to addresses within the dual-port RAM, providing single-cycle as opposed to dual-cycle access to these more commonly addressed locations.

The 1553 interface will provide no direct control of any board function, communicating only with the dual-port RAM. All board functions will be controlled by data values written to the RAM which cause the local microcontroller to perform control activities.

Dual-Port SRAM

Approximately 66K locations of eight-bit wide dual-port SRAM are provided. 64K of these form a Sector Shadow Buffer equivalent to one sector of Flash RAM, allowing the 1553 interface to load new data into the Flash one sector at a time. The remaining 4K locations provide the control interface to the microcontroller as described in John Anderson's notes found at http://d0server1/users/janderson/Public~1/a980922a.pdf. The microcontroller polls locations in the dual-port SRAM for commands and leaves board status data at other locations for 1553 to read as desired.

PIC14000 Microcontroller

The microcontroller is responsible for taking the various DAC settings found in the dual-port RAM and loading them into the octal DACs that control the MCM. In addition, the microcontroller has a built-in Wilkenson ADC which allows digitzation and verification of the DAC outputs and other board analog signals. The microcontroller also oversees the use of the Flash RAM and automatically performs a download of the Flash RAM data into the Altera FPGA on board every time power is applied. While the board is in use, new FPGA programs may be downloaded through the dual-port RAM into the Flash RAM, and upon request, the microcontroller will reprogram the FPGA from this new data.

Helper CPLD

The Helper CPLD provides some decoding logic for the microcontroller and assists in the transfer of large data blocks between the dual-port RAM, the Flash RAM and the FPGA.

DACs and Analog Mux

The DACs and anaog mux, more completely described in the documentation found at http://d0server1/users/janderson/Public~1/a980916a.pdf, provide the various control voltages necessary for the operation of the SIFT in the MCM. Through programmed voltages generated by the DACs, the gain and threshold of the SIFT may be set as desired. The Analog Mux provides a convenient method to check that all the DACs are working by providing a programmable feedback path to the ADC in the microcontroller.

Flash RAM

An AMD Flash RAM is used to store, in a nonvolatile form, the logic implemented in the Altera FPGA. Upon power up or reset the contents of the Flash are copied into the FPGA. New data may be stored in the Flash by loading it into the dual-port RAM, and asking the microcontroller to reprogram the Flash part. Verification of Flash data is performed by asking the microcontroller to copy one sector of Flash into the Sector Shadow Buffer in the dual-port RAM.

Altera FPGA

This FPGA connects to all 72 discriminator outputs of the SIFT and may be used to emulate part of the track finding logic which will be implemented in the CFT Axial board. The FPGA also connects to various other signals within the test board and may be used to provide oscilloscope or logic analyzer trigger outputs. A couple of headers are provided at the outputs of the FPGA for convenient connection of a logic analyzer.

I/O Connections

This section will be updated as we agree on the various links.